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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
CAMPOS, YAIMA

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,355	HSIEH, HSIANG-AN	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The examiner acknowledges the applicant's submission of the amendment dated June 16, 2006. At this point claims (1, 2, 5 and 11) have been amended, and claim 3 has been cancelled. Thus, claims (1-2 and 4-16) are pending in the instant application.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections – 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claim 1** is rejected under 35 U.S.C. 102(e) as being anticipated by Chou et al. (US 2005/0055481).

3. As per **claim 1**, Chou discloses "A card reader connected between an external system side and a silicon storage device," as **["this invention relates to flash-memory drives/readers" (Column 1, paragraph 0001, lines 1-2) Figure 4 shows "flash memory 36" which comprises a silicon storage device, "Flash drive controller chip 65" which comprises a "card reader" and "usb 18" which is used for "uploading the data to a PC or other device" which comprises an external system (Column 2, Paragraphs 0026-0029) (See Figures 4-7)]** "comprising: a silicon storage device connector, electrically coupled to a silicon storage device;" **[With respect to this limitation, Chou discloses "The flash drive/reader of FIGS. 1, 2 can be**

connected to USB link 128 of the PC in FIG. 3" (Column 1, paragraph 0011, lines 2-3). Figure 4 shows "flash memory 36" which comprises a silicon storage device, "Flash drive controller chip 65" which comprises a "card reader" and "usb 18" which is used for "uploading the data to a PC or other device" which comprises an external system (Column 2, Paragraphs 0026-0029) (See Figures 4-7)] "and a bridge controller, electrically coupled to the silicon storage device connector, wherein when the bridge controller receives a read instruction, the bridge controller prefetches a part of data requested by the read instruction from the silicon storage device in advance, and saves the part of data in the bridge controller" **[Chou discloses this limitation as "prefetching of flash data may be performed by flash-memory controller 30 (Figs. 4,6) or by flash-card controllers 50,54 (Figs. 5,7) writing additional pages of flash data to the RAM buffer. For example, m blocks of flash data may be pre-fetched, where m can be a programmable number of pages to pre-fetch ahead of the current page being read" (Column 3, paragraph 0045). To further explain, Applicant should note arrangement of Figures 4-6 which comprises connectors/connections coupling an external system to a card reader and a card reader to a memory card and different connectors coupling the internal components of memory card reader such as "flash controller" to "ram buffers" and to "flash memory"].**

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2 and 4-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wurzburg (US 2005/0097263) in view of Chou (US 2005/0055481).

6. As per **claim 2**, Wurzburg discloses "A bridge controller, embedded in a card reader electrically coupling to a silicon storage device and an external system side," as **["the invention comprises a system and method for designing a flash memory card reader to IDE Bridge (IDE-CR Bridge) to create and interface between a flash-memory card-reader and an IDE controller. The IDE controller may be comprised in an embedded system" (Column 2, paragraph 0019)]** "comprising: a microprocessor;" **[With respect to this limitation, Wurzburg discloses that "embedded system 10 includes a microprocessor 12" (Column 2, paragraph 0020, line 4)]** "a silicon storage device interface, accessing said silicon storage device according to instruction of the microprocessor;" **[With respect to this limitation, Wurzburg discloses that "the invention comprises a flash-memory card reader to Integrated Drive Electronics (IDE) Bridge (or interface)" (Column 1, paragraph 0010, lines 2-3) and explains that "the internal microprocessor and its program convert the IDE/ATA commands and status/data requests into the formats used by each of the four basic types of Flash Card media" (Column 1, paragraph 0010, lines 13-16)]** "a system interface, receiving data transferred from buffers respectively according to instruction of said microprocessor;" **[With respect to this limitation, Wurzburg discloses "IDE/ATA interface (IAI)" and explains that "IAI 102 may receive IDE/ATA commands from an IDE controller configured in a host system, (for example IDE controller 22, as illustrated in Fig. 1). The data may be buffered in TRB 104 (*transmit/receive buffer*)" (Column 2, paragraph 0021)]** "a transmission buffer, electrically coupled to said silicon storage device interface and said system

interface;" **[Wurzburg discloses this limitation as "an IDE/ATA interface (IAI) 102 is coupled to a transmit/receive buffer (TRB) 104 and an ATA command/status register emulation buffer (CSRB)" (Column 2, paragraph 0021)]** "an allocation table buffer, electrically coupled to said system interface and said silicon storage device interface for storing a data accessing address mapping table" **[Wurzburg discloses this concept in "Fig. 2 illustrates a schematic diagram of one embodiment of IDE-CRs" including "an ATA command/status register emulation buffer (CSRB) 106" which equivalent to an allocation table buffer as it "translates the IDE/ATA command and status information into control and status information of a format used by a flash-memory card type corresponding to the device currently being processed by the IDE controller" wherein "An address and data bus 160 may couple CSRB 106 and MP 108, enabling data transfer between MP 108, CSRB 106 and a flash media controller (FMC) unit 110 interfacing with the actual flash-memory cards for exchanging commands/status information" (Column 2, paragraphs 0021 and 0023) and also discloses that "Generally, flash-memory card media is very similar to hard disk drives (HDDs) in that flash-memory cards are usually formatted in a Windows file format, such as File Allocation Table (FAT) or NT File System (NTFS)" (Column 1, paragraph 0010). Applicant should note that command/status/data translation is commonly known in the art to comprise address translation, mapping and interpretation and that when write accesses/commands are made to memory, the status of data in memory changes and must be updated].**

Wurzburg does not disclose expressly "a cache buffer, overlapping said transmission buffer to couple with said silicon storage device interface and said system interface; wherein,

when said microprocessor outputting a read instruction, one of said buffers transferring alternatively to the system interface."

Chou discloses the concept of having "a cache buffer, overlapping said transmission buffer to couple with said silicon storage device interface and said system interface; wherein, when said microprocessor outputting a read instruction, one of said buffers transferring alternatively to the system interface" as **["the present invention relates to flash-memory drives/readers" (Column 1, paragraph 0001) wherein "prefetching of flash data may be performed by flash-memory controller 30 (Figs. 4,6 or by flash-card controllers 50,54 (Figs. 5,7) writing additional pages of flash data to the RAM buffer" (Column 3, paragraph 0045) which is equivalent to a transmission buffer. Chou explains that "additional RAM buffers could be added, or the RAM buffer could be partitioned to allow simultaneous access without arbitration delays of different memory partitions" (Column 4, paragraph 0054) and further teaches an embodiment having "a flash drive with external and internal RAM buffers. Most of the components of the flash drive could be integrated into a single integrated circuit (IC) chip 68" wherein "external RAM buffer 60" is provided "when larger blocks of data are stored, the overflow data is stored in external RAM buffer 60" (Column 3, paragraphs 0037 and 0038) which is equivalent to having a cache buffer to overlap a transmission buffer, as claimed by Applicant. Chou explains that "either internal RAM buffer 34 or external RAM buffer 60 can be accessed through flash-serial buffer bus 40" (Column 3, paragraph 0038, lines 7-9). Applicant should note that if both, the internal and external RAM buffers are holding data, only the buffer holding data requested by a read command will provide this data]**. Chou also discloses the concept of an address-mapping

table analogous to "an allocation buffer, electrically coupled to said system interface and said silicon storage device interface for storing a data accessing address mapping table" as **["Rather than use FIFO buffers, the flash data can be stored out of sequence. A catalog or index can be used to locate the desired pages, or other address remapping or translation logic may be used" (Column 4, paragraph 0054) which is also equivalent to having allocation table buffer storing an allocation mapping table. Applicant should further note that a mapping table is addressed or updated every time a write access is made to memory]**.

Wurzburg (US 2005/0097263) and Chou (US 2005/0055481) are analogous art because they are from the same field of endeavor of memory card access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the memory card reader which includes a transmission buffer as taught by Wurzburg and further include an additional cache buffer that overlaps the transmission buffer to receive/output read data alternatively as taught by Chou.

The motivation for doing so would have been because Chou teaches that including and additional cache buffer that overlaps the transmission buffer to receive/output read data alternatively **[allows transferring of larger amounts of data as "buffering of the data during the transfer between the flash-memory controller and the serial engine can improve throughput" (Column 2, paragraph 0025). Chou also discloses that "additional RAM buffers could be added, or the RAM buffer could be partitioned to allow simultaneous access without arbitration delays of different memory partitions" (Column 4, paragraph 0054)]**.

Therefore, it would have been obvious to combine Chou (US 2005/0055481) with Wurzburg (US 2005/0097263) for the benefit of creating a memory card reader to obtain the invention as specified in claim 2.

7. As per **claim 4**, the combination of Wurzburg and Chou discloses "The bridge controller of claim 2," **[See rejection to claim 2 above]** and claim 4 further requires:

"means for transmitting data transmission operation is alternately and synchronously performed between said cache buffer and said transmission buffer" **[(*Page 19, paragraph 0042 of applicant's specification identifies these means as "cache buffer 120" and "transmission buffer 118"*) [With respect to this limitation, Chou discloses "internal RAM buffer" and "external RAM buffer" (Column 3, paragraphs 0037-0038) and explains that "Since RAM buffer 34, flash-memory controller 30, and serial engine 32 each have two ports, one for each of buses 38, 40, concurrent accesses can occur" (Column 2, paragraph 0032) as having concurrent/synchronous transmission operations. Applicant should note that if both, the internal and external RAM buffers are holding data, only the buffer holding data requested by a read command will provide this data].**

8. As per **claims 5 and 11**, Wurzburg discloses "A method for data transmission of a card reader," as **["the invention comprises a system and method for designing a flash memory card reader to IDE Bridge (IDE-CR Bridge) to create and interface between a flash-memory card-reader and an IDE controller. The IDE controller may be comprised in an embedded system" (Column 2, paragraph 0019)"]** "wherein said card reader comprising a transmission buffer," **[Wurzburg discloses this limitation as "an IDE/ATA interface (IAI) 102 is coupled to a transmit/receive buffer (TRB) 104 and an ATA command/status register**

emulation buffer (CSRB)" (Column 2, paragraph 0021)] "a system interface" **[With respect to this limitation, Wurzburg discloses "IDE/ATA interface (IAI)" and explains that "IAI 102 may receive IDE/ATA commands from an IDE controller configured in a host system, (for example IDE controller 22, as illustrated in Fig. 1). The data may be buffered in TRB 104 (*transmit/receive buffer*)" (Column 2, paragraph 0021)]** "and a silicon storage device interface," **[With respect to this limitation, Wurzburg discloses that "the invention comprises a flash-memory card reader to Integrated Drive Electronics (IDE) Bridge (or interface)" (Column 1, paragraph 0010, lines 2-3) and explains that "the internal microprocessor and its program convert the IDE/ATA commands and status/data requests into the formats used by each of the four basic types of Flash Card media" (Column 1, paragraph 0010, lines 13-16)]**"said method comprising: receiving a first data requested by a read instruction, wherein said first data is received by said transmission buffer;" **[Wurzburg discloses this limitation as "FIG. 2 illustrates a schematic diagram of one embodiment of IDE-CR Bridge 26. In this embodiment, an IDE/ATA interface (IAI) 102 is coupled to a transmit and receive buffer (TRB) 104 and an ATA command/status register emulation buffer (CSRB) 106. IAI 102 may receive IDE/ATA commands and data from an IDE controller configured in a host system, (for example IDE controller 22, as illustrated FIG. 1). The data may be buffered in TRB 104" (Column 2, paragraph 0021)]** "an allocation table buffer" wherein "the receipt of the first data is performed through a data accessing address mapping table stored in the allocation buffer" **[Wurzburg discloses this concept in "Fig. 2 illustrates a schematic diagram of one embodiment of IDE-CRs" including "an ATA command/status register emulation buffer (CSRB) 106" which equivalent to an allocation**

table buffer as it "translates the IDE/ATA command and status information into control and status information of a format used by a flash-memory card type corresponding to the device currently being processed by the IDE controller" wherein "An address and data bus 160 may couple CSRB 106 and MP 108, enabling data transfer between MP 108, CSRB 106 and a flash media controller (FMC) unit 110 interfacing with the actual flash-memory cards for exchanging commands/status information" (Column 2, paragraphs 0021 and 0023) and also discloses that "Generally, flash-memory card media is very similar to hard disk drives (HDDs) in that flash-memory cards are usually formatted in a Windows file format, such as File Allocation Table (FAT) or NT File System (NTFS)" (Column 1, paragraph 0010). Applicant should note that command/status/data translation is commonly known in the art to comprise address translation, mapping and interpretation].

Wurzburg does not disclose having "a cache buffer," and "storing a second data predetermined by said read instruction into either said cache buffer or said transmission buffer when either buffer is approaching full status; and outputting sequentially said data stored in said transmission buffer and said cache buffer."

Chou discloses having "a cache buffer," and "storing a second data predetermined by said read instruction into either said cache buffer or said transmission buffer when either buffer is approaching full status; and outputting sequentially said data stored in said transmission buffer and said cache buffer." **[With respect to these limitations, Chou discloses ["the present invention relates to flash-memory drives/readers" (Column 1, paragraph 0001) wherein "prefetching of flash data may be performed by flash-memory controller 30 (Figs. 4,6 or by flash-card controllers 50,54 (Figs. 5,7) writing additional pages of flash data to the RAM**

buffer" (Column 3, paragraph 0045) which is equivalent to a transmission buffer or a cache buffer. Chou explains that "additional RAM buffers could be added, or the RAM buffer could be partitioned to allow simultaneous access without arbitration delays of different memory partitions" (Column 4, paragraph 0054) and further teaches an embodiment having "a flash drive with external and internal RAM buffers. Most of the components of the flash drive could be integrated into a single integrated circuit (IC) chip 68" wherein "external RAM buffer 60" is provided "when larger blocks of data are stored, the overflow data is stored in external RAM buffer 60" (Column 3, paragraphs 0037 and 0038) which is equivalent to having a second buffer in addition to a first buffer, as claimed by Applicant. Chou explains that "either internal RAM buffer 34 or external RAM buffer 60 can be accessed through flash-serial buffer bus 40" (Column 3, paragraph 0038, lines 7-9). Applicant should note that if both, the internal and external RAM buffers are holding data, only the buffer holding data requested by a read command will provide this data. Chou further specifies that "Once one or more blocks of flash data have been written into RAM buffer 34 by flash-memory controller 30, serial engine 32 can read the flash data and serially transmit the flash data over USB link 18, uploading the data to a PC or other device" (Column 2, paragraph 0027)]. Chou further discloses the concept of having)] "an allocation table buffer" wherein "the receipt of the first data is performed through a data accessing address mapping table stored in the allocation buffer" as **["Rather than use FIFO buffers, the flash data can be stored out of sequence. A catalog or index can be used to locate the desired pages, or other address remapping or translation logic may be used" (Column 4, paragraph 0054) which is also analogous to having allocation table buffer**

storing an allocation mapping table. Applicant should note that a mapping table is addressed or updated every time a write access is made to memory; which comprises receiving data].

Wurzburg (US 2005/0097263) and Chou (US 2005/0055481) are analogous art because they are from the same field of endeavor of memory card access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the memory card reader which includes a transmission/first buffer as taught by Wurzburg and further include an additional cache/second buffer to store read data when the either buffer is approaching full status as taught by Chou.

The motivation for doing so would have been because Chou teaches that including and additional buffer to store read data when a first buffer is approaching full status **[allows transferring of larger amounts of data as "buffering of the data during the transfer between the flash-memory controller and the serial engine can improve throughput" (Column 2, paragraph 0025). Chou also discloses that "additional RAM buffers could be added, or the RAM buffer could be partitioned to allow simultaneous access without arbitration delays of different memory partitions" (Column 4, paragraph 0054)]**.

Therefore, it would have been obvious to combine Chou (US 2005/0055481) with Wurzburg (US 2005/0097263) for the benefit of creating a memory card reader to obtain the invention as specified in claims 5 and 11.

9. As per **claims 6 and 12**, the combination of Wurzburg and Chou discloses "The method as cited in claims 5 and 11," **[See rejection to claims 5 and 11 above]** "said method further comprising a step for comparing said data stored in said buffers following said step of storing

said second data, wherein said comparison step determining the first position of said second data following the last position of said first data" **[Chou discloses this concept as it is taught that "the flash controller can then pre-fetch another m pages from the new current location. The write pointer is set to the end of the page being read, or to the end of the block of pre-fetched data includes the page being read by the serial engine" (Column 3, paragraph 0047). Applicant should note that if a pointer is placed at the end of a first pre-fetched block of data, the position for any new/second data to be prefetched will follow the last position of the first data. Chou also explains; "hardware comparators of other logic can be used to detect full and empty conditions. The CPU can write the starting and ending locations, allowing CPU to adjust memory allocations for read and write buffers" (Column 3, paragraph 0044)]**.

10. As per **claims 7 and 13**, the combination of Wurzburg and Chou discloses "The method as cited in claims 5 and 11," **[See rejection to claims 5 and 11 above]** "further comprising: removing said data from said transmission buffer and said cache buffer after outputting said data" **[Chou discloses this limitation as "when the serial engine causes the read pointer to move past old pre-fetched data, the old data is discarded" (Column 4, paragraph 0049)]**.

11. As per **claims 8 and 14**, the combination of Wurzburg and Chou discloses "The method as cited in claims 5 and 11," **[See rejection to claims 5 and 11 above]** "wherein said method is alternately and synchronously performed to transmit data" **[With respect to this limitation, Chou discloses that "Since RAM buffer 34, flash-memory controller 30, and serial engine 32 each have two ports, one for each of buses 38, 40, concurrent accesses can occur" (Column 2, paragraph 0032) as having concurrent/synchronous transmission operations.**

Applicant should note that if both, the internal and external RAM buffers are holding data, only the buffer holding data requested by a read command will provide this data].

12. As per **claims 9 and 15**, the combination of Wurzburg and Chou discloses "The method as recited in claims 5 and 11" **[See rejection to claims 5 and 11 above]** "said card reader further comprising an allocation table buffer, and said method writing a data accessing address mapping table into said allocation table buffer;" **[With respect to this limitation, Wurzburg discloses; "Fig. 2 illustrates a schematic diagram of one embodiment of IDE-CRs" including "an ATA command/status register emulation buffer (CSRB) 106" wherein "An address and data bus 160 may couple CSRB 106 and MP 108, enabling data transfer between MP 108, CSRB 106 and a flash media controller (FMC) unit 110 interfacing with the actual flash-memory cards for exchanging commands/status information" (Column 2, paragraph 0021) and also discloses that "Generally, flash-memory card media is very similar to hard disk drives (HDDs) in that flash-memory cards are usually formatted in a Windows file format, such as File Allocation Table (FAT) or NT File System (NTFS)" (Column 1, paragraph 0010)]**. Chou also discloses having an address-mapping table as **["Rather than use FIFO buffers, the flash data can be stored out of sequence. A catalog or index can be used to locate the desired pages, or other address remapping or translation logic may be used" (Column 4, paragraph 0054)]** "updating content of said data accessing address mapping table with a written data according to a write instruction; writing said written data into said silicon storage device through said silicon storage device interface from said cache buffer according to said content updated of said data accessing address mapping table; and writing said data accessing address mapping table into said silicon storage device after

completion of writing operation into said silicon storage device" as **[With respect to this limitation Wurzburg discloses that "transfer of commands (translated by MP (*microprocessor*)108) between MP 108 and flash-memory card controllers may take place through control" wherein "Outgoing commands/status/data generated by the flash-memory card controller may be translated into hard disk commands/status/data usable by the hard disk controller (310), and those hard disk commands/status/data may be provided to the hard disk controller (312). The outgoing commands/status may be generated in response to the incoming commands/status and may comprise read and/or write commands" (Column 3, paragraphs 0022 and 0023) as having read/write commands and translation/decoding means for microprocessor instructions. Chou also explains and embodiment wherein a FIFO buffer and a pointer are used for address mapping, having functionality equivalent to Applicant's claimed invention wherein "FIGS. 9A, B show flash-data buffers in the RAM buffer. FIFO buffers can be used for read and write data. FIG. 9A shows write buffer 160 that stores data to be written into a flash memory. Starting and ending locations of write buffer 160 in the RAM buffer can be indicated by start location ST_WB and end location END_WB. The current location for the serial engine to write the next word or block of flash data is pointed to by pointer W_WB_PTR, while the next location for the flash controller to read from is indicated by R_WB_PTR. These pointers are advanced when data is read or written. The pointers can wrap around at the end of write buffer 160. When the write pointer reaches the read pointer the buffer is full and can accept no more data. When the read pointer reaches the write pointer the buffer is empty. Active write-buffer data 162 is the valid data between the two pointers" (Column 3,**

paragraph 0042); further explains that "blocks or pages of flash memory can be stored in a variety of arrangements" (Column 3, paragraph 0043) wherein "Rather than use FIFO buffers, the flash data can be stored out of sequence. A catalog or index can be used to locate the desired pages, or other address remapping or translation logic may be used" (Column 4, paragraph 0054) as specifying that addressing/mapping data may be stored in a table/index form in a buffer instead of using pointers to read/write data to buffers].

13. As per **claims 10 and 16**, the combination of Wurzburg and Chou discloses "The method as cited in claims 9 and 15," **[See rejection to claims 9 and 15 above]** "wherein said step of writing said written data into said silicon storage device through said silicon storage device interface from said cache buffer processing simultaneously with decoding data of said microprocessor" **[With respect to this limitation, Wurzburg discloses "transfer of commands (translated by MP (*microprocessor*)108) between MP 108 and flash-memory card controllers may take place through control" wherein "Outgoing commands/status/data generated by the flash-memory card controller may be translated into hard disk commands/status/data usable by the hard disk controller (310), and those hard disk commands/status/data may be provided to the hard disk controller (312). The outgoing commands/status may be generated in response to the incoming commands/status and may comprise read and/or write commands" (Column 3, paragraphs 0022 and 0023) as having read/write commands and translation/decoding means for microprocessor instructions].**

II. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

14. Applicant's arguments filed on June 16, 2006 have been fully considered but they are not deemed to be persuasive and, as required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

III. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1st POINT OF ARGUMENT:

15. Regarding Applicant's remark that Chou does not disclose "a silicon storage device connector, electrically coupled to the silicon storage device," it is the Examiner's position that due to the bread of the claim language, Chou's disclosure meets this limitation **[(See rejection to claim 1 above; Figures 4-6) wherein Figure 4 shows "flash memory 36" which comprises a silicon storage device, "Flash drive controller chip 65" which comprises a "card reader" and "usb 18" which is used for "uploading the data to a PC or other device" which comprises an external system (Column 2, Paragraphs 0026-0029) (See Figures 4-7). Applicant should note arrangement of Figures 4-6 which comprises connectors/connections coupling an external system to a card reader and a card reader to a memory card and different connectors coupling the internal components of memory card reader such as "flash controller" to "ram buffers" and to "flash memory"]**.

2ND POINT OF ARGUMENT:

16. Regarding Applicant's remark that in the combination of Wurzburg and Chou, "RAM buffer 34" and "RAM buffer 60" are not integrally connected because they can be interrupted by a switch so as not to be able to achieve a purpose of storing overflow data in the external RAM 60, it is the examiner's position that this limitation is not reflected in the claims.

3rd POINT OF ARGUMENT:

17. Regarding Applicant's remark that the Wurzburg and Chou combination does not disclose "a cache buffer, overlapping said transmission buffer," it is the Examiner's position that the combination of Wurzburg and Chou discloses this limitation **(See rejection to claim 2 above)**. Furthermore, even though Chou uses different names or labels for "cache buffer" and "transmission buffer," the "RAM 60" and "RAM 34" perform the same function as the claimed "cache buffer" and "transmission buffer". The different names/labels does not distinguish Applicant's invention over the prior art.

4th POINT OF ARGUMENT:

18. Regarding Applicant's remark that the Wurzburg and Chou combination does not disclose "an allocation table buffer, electrically coupled to said system interface and said silicon storage device interface for storing a data accessing address mapping table," and "the receipt of the first data is performed through a data accessing address mapping table stored in the allocation table buffer" it is the Examiner's position that the combination of Wurzburg and Chou discloses this concept as **[Wurzburg discloses this concept in "Fig. 2 illustrates a schematic diagram of one embodiment of IDE-CRs" including "an ATA command/status register emulation**

buffer (CSRB) 106" which equivalent to an allocation table buffer as it "translates the IDE/ATA command and status information into control and status information of a format used by a flash-memory card type corresponding to the device currently being processed by the IDE controller" wherein "An address and data bus 160 may couple CSRB 106 and MP 108, enabling data transfer between MP 108, CSRB 106 and a flash media controller (FMC) unit 110 interfacing with the actual flash-memory cards for exchanging commands/status information" (Column 2, paragraphs 0021 and 0023) and also discloses that "Generally, flash-memory card media is very similar to hard disk drives (HDDs) in that flash-memory cards are usually formatted in a Windows file format, such as File Allocation Table (FAT) or NT File System (NTFS)" (Column 1, paragraph 0010). Applicant should note that command/status/data translation is commonly known in the art to comprise address translation, mapping and interpretation and that when write accesses/commands are made to memory, the status of data in memory changes and must be updated]. Chou also discloses this concept as **["Rather than use FIFO buffers, the flash data can be stored out of sequence. A catalog or index can be used to locate the desired pages, or other address remapping or translation logic may be used" (Column 4, paragraph 0054) which is also equivalent to having allocation table buffer storing an allocation mapping table. Applicant should further note that a mapping table is addressed or updated every time a write access is made to memory]**.

19. All arguments by the applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated June 16, 2006.

IV. CLOSING COMMENTS

Conclusion

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

V. STATUS OF CLAIMS IN THE APPLICATION

21. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

22. Per the instant office action, claims **1-2 and 4-16** have received a second action on the merits and are subject of a final rejection.

CLAIMS NO LONGER IN THE APPLICATION

23. Claim 3 was cancelled by the amendment dated June 16, 2006.

24. For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

VI. DIRECTION OF FUTURE CORRESPONDENCES

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232 and email address is Yaima.Campos@uspto.gov. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

26. If attempts to reach the above noted Examiner by telephone or email are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098.

27. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 14, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
PRIMARY EXAMINER